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(54) Display device.

(57) A liquid crystal display has a matrix of pixels 1 each with a continuously clocked counter 2, used both as the data store and as the mechanism of grey scale generation. The grey level of each pixel 1 is stored as the phase of the counter 2 with respect to a reference count.

The data bus 3, load clock 4, counter clock 5 and master phase reference 6 are all lines which transport signals common to a large number of pixels.

The shift data line 7 is used to propagate a bit which enables the counter load input. Each pixel circuit instructs the adjacent circuit that it is next to be loaded, by use of a clock delay 8. Thus pixels are loaded in sequence from data on the load bus 3, that data being changed between load clock pulses. The bistable circuit element 9, set from the master timing and reset from the counter, has an output which directly drives a bistable liquid crystal display device 10.

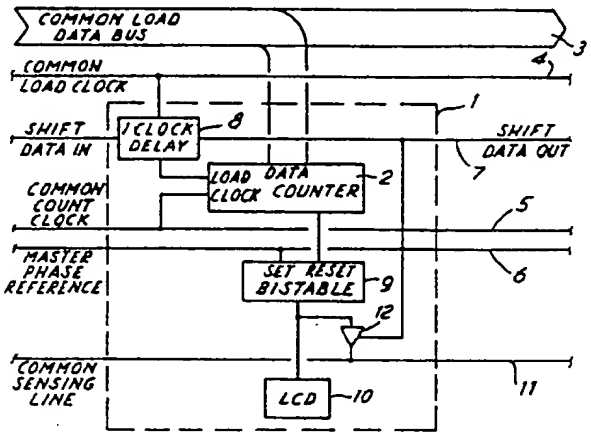

FIG. 1

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DISPLAY DEVICE

The present invention relates to a display device, and especially, but not solely, to a grey-scale television display using bistable elements, for example made from ferroelectric liquid-crystal material.

British Patent Specification Publication No. 2047453A discloses a L.E.D. or gas discharge matrix addressed by rows, the columns being driven by amplitude and duration-modulated current. For each column a counter is loaded with a number representing the required brightness and counted down to zero. Each counter stage operates a gate which controls a weighted current.

The present invention provides a display device comprising:

a lattice of pixels;

each pixel having a counter operable for continuous counting; and

means to operate one or more counters to effect actuation of each pixel for a time duration within each picture in accordance with the value of the picture-signal for that pixel.

Preferably a pixel is actuated for a time period corresponding to the interval between the reception, at the pixel, of a specified characteristic (e.g. a change of bit state) in the picture-signal and the occurrence of that specified characteristic in a reference signal.

Thus preferably, a counter has means to monitor for the presence of a specified characteristic in an input signal, and means to set the associated pixels to a state upon detection of the specified characteristic. Preferably, the display device has means to input a signal to pixels in order to set each said pixel to a state.

Another aspect of the present invention provides a method of operating a display device comprising a lattice of pixels, each having a counter operable for continuous counting, the method comprising operating counters to effect actuation of each pixel for a time duration in accordance with the value of the picture-signal for that pixel.

Preferably, a pixel is actuated for a time period corresponding to the interval between the reception, at the pixel, of a specified characteristic in the picture-signal and the occurrence of that specified characteristic in a reference signal.

Preferably, a counter is monitored for the presence of a specified characteristic in an input signal, and setting the associated pixels to a state upon detection of the specified characteristic.

Preferably in the invention, a pixel comprises one or more liquid crystal cells.

The invention is applicable to colour displays and to monochrome displays.

The present invention also embodies equipment for the generation, and/or transmission, and/or reception, and/or processing, of signals suited and/or designed for a display device as herein defined.

In order that the invention may more readily be understood, a description is now given, by way of example only, reference being made to the accompanying drawings, in which:-

Figure 1 is a circuit diagram of a pixel within a display device embodying the present invention;

Figure 2 is a representation of the waveforms of the circuit of Figure 1;

Figure 3 is a representation of the waveforms for a modified circuit diagram,

Figure 4 is a circuit diagram of part of a pixel within a ferroelectric liquid crystal display embodying the present invention;

Figure 5 is a representation of the waveforms of Figure 4;

Figure 6 is a graph of transmission against r.m.s. applied voltage for another form of liquid crystal display; and

Figure 7 is a representation of the waveforms for the display of Figure 6.

In the pixel 1 of Figure 1, a continuously clocked counter 2 is used both as the data store and as the mechanism of grey scale generation, in order to minimise circuit size and complexity. Because the counter 2 is continuously clocked, it can use dynamic circuitry which takes up less silicon area. The grey level of each pixel 1 is stored as the phase of the counter 2 (i.e. the phase of the counter's most significant bit) with respect to a reference count. The phase is controlled by loading each counter with a value representing the grey level, as the television signal is received. If each bistable pixel 1 passes light for the time difference between its counter's phase and the reference phase, the result is a grey level display as required.

The data bus 3, load clock 4, counter clock 5 and master phase reference 6 are all lines which transport signals common to a large number of pixels; therefore although they must be buffered at some point in the circuit, that might only be every 50 elements, so that the only space taken up by these signals is in interconnections.

The shift data line 7 is used to propagate a bit which enables the counter load input. In effect each pixel circuit instructs the adjacent circuit that it is next to be loaded, by use of a clock delay 8. Thus pixels are loaded in sequence from data on the load bus 3, that data being changed between load

clock pulses. The bistable circuit element 9, set from the master timing and reset from the counter, has an output which directly drives a bistable liquid crystal display device 10.

Figure 2 shows some timing waveforms to go with Figure 1. The counter clock and the load clock have been drawn separately in Figure 1 to emphasise that there is no relationship between them. Indeed, if the data input is halted completely, the counters would continue clocking indefinitely, displaying the grey scale image that is stored as phase information. In practice the load clock is determined by the picture input rate, while the counter clock is arranged so that the counter recycles above the flicker fusion frequency, for instance, the counter might cycle twice per television field.

A common sensing line 11 is fed from a tristate driver 12 at each pixel, the tristate driver 12 being active at whichever pixel was last loaded with data. This allows the counter phase to be monitored remotely, which is a check on the operation of the total circuit at that pixel. By continuing to monitor the sensing line, while loading successive counters with data, the operation of each pixel circuit may be checked in turn.

In one arrangement, a counter 2 has one stage more than the number of data bits e.g. for a 4-bit word giving 16 grey levels, the bits are loaded into the four least significant stages of a 5 stage counter. A similar counter is used to generate the master phase reference which sets the bi-stable each time the MSB changes, namely every 16 counter clock pulses. If a pixel counter is loaded with a value N and counted down, the M.S.B. changes after N, N + 16, N + 32 (and so on) clock pulses and re-sets the bi-stable. Therefore if the counter is loaded when the master counter is in a reference phase (for example immediately after the MSB has changed state and set the bi-stable), the bi-stable remains in the set state for N clock periods. It is necessary for all the counters using the same master reference phase to be loaded during one period of the counter clock as well as at a specific phase of the master counter.

In a modification, instead of an electronic gating signal as in Figure 1, the pixel 1 is driven directly by the square wave from the counter output, while the gating is performed by switching on and off the light source. Figure 3 shows timing diagrams for this arrangement. One advantage is that, as long as the image is static, each pixel 1 is switched on and off for equal times, so has no opportunity to build up a memory of the grey level state it is in. A second advantage is that, if the light source can be switched sequentially to red, green, and blue, a colour display can be produced without the need for separate pixels. It is necessary to have separate counters for the red, green, and blue components, so as to control each pixel sequentially, in synchronism with the changes in the light source.

The pixel drive voltage depends on the display material used, as does the optimum waveform to be used for driving. For instance, if the LCD is of ferroelectric material, the waveform of Figure 2 is not directly suitable, since it contains a d.c. component. One solution is to a.c. couple the signal by depositing a thin insulating layer on the display plate to act as a capacitor 20 in series with each ferroelectric liquid crystal device 21 (see Figure 4). The pixel is then switched by the edge spikes of the waveform, assuming that it has a low enough internal resistance to charge up the series capacitor between edges. Figure 5 shows the waveforms for this arrangement.

In another modification, suitable for driving twisted nematic, guest-host, or similar liquid crystal, the back electrode of each pixel is driven directly by the most significant bit of the counter, while the front electrode is driven by the reference square wave. The reference square wave has the same frequency as the counter output, but not necessarily the same phase, while its amplitude may be the same or somewhat greater than the amplitude of the counter output. If all the pixels in the image have the same reference square wave, the front of the screen may conveniently be driven as a single electrode.

Figure 6 shows schematically the transmission of a guest-host liquid crystal cell as a function of the rms applied voltage. RMS voltages between V1 and V2 are needed to control the cell brightness. Figure 7 shows an example of the voltages applied to the electrodes of one LCD pixel according to the invention, together with the voltage across the pixel. As the phase of the back electrode drive is altered the RMS drive across the pixel can in this case be varied between 1 and 6 volts.

In general, if the back electrode square wave is Vb volts rms (2Vb peak to peak) and the front electrode square wave is Vf volts rms, then by varying the phase of the back electrode drive the rms voltage across the cell can be controlled between (Vf -Vb) and (Vf + Vb).

Claims

1. A display device comprising:
a lattice of pixels;
each pixel having a counter operable for continuous counting; and
means to operate one or more counters to

effect actuation of each pixel for a time duration in accordance with the value of the picture-signal for that pixel.

2. A display device according to Claim 1, wherein a pixel is actuated for a time period corresponding to the interval between the reception, at the pixel, of a specified characteristic in the picture-signal and the occurrence of that specified characteristic in a reference signal.

3. A display device according to Claims 1 or 2, wherein a counter has means to monitor for the presence of a specified characteristic in an input signal, and means to set the associated pixels to a state upon detection of the specified characteristic.

4. A display device according to any one of the preceding Claims, wherein the display device has means to input a signal to pixels in order to set each said pixel to a state.

5. A display device according to any one of the preceding Claims, wherein liquid crystal cells form the lattice.

6. A method of operating a display device comprising a lattice of pixels, each having a counter operable for continuous counting, the method comprising operating counters to effect actuation of each pixel for a time duration in accordance with the value of the picture-signal for that pixel.

7. A method according to Claim 6, wherein a pixel is actuated for a time period corresponding to the interval between the reception, at the pixel, of a specified characteristic in the picture-signal and the occurrence of that specified characteristic in a reference signal.

8. A method according to Claim 6 or 7, comprising monitoring a counter for the presence of a specified characteristic in an input signal, and setting the associated pixels to a state upon detection of the specified characteristic.

9. A method according to any one of Claims 6 to 8, comprising inputting a signal to pixels in order to set each said pixel to a state.

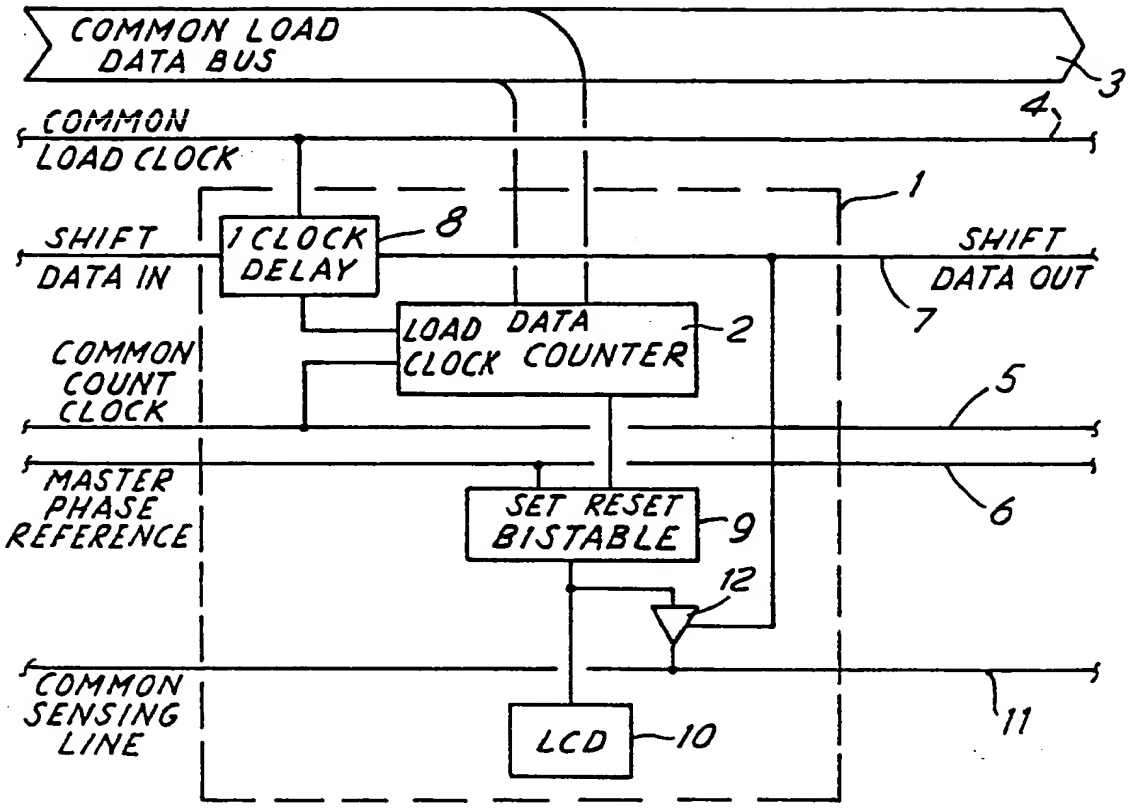

FIG. 1

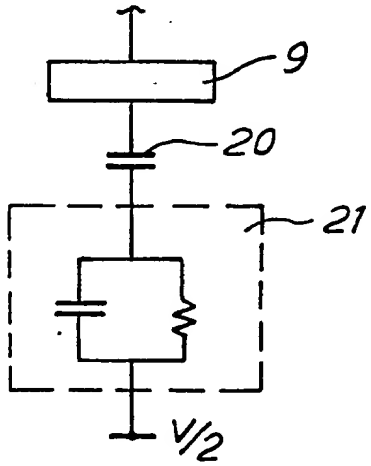

FIG. 4

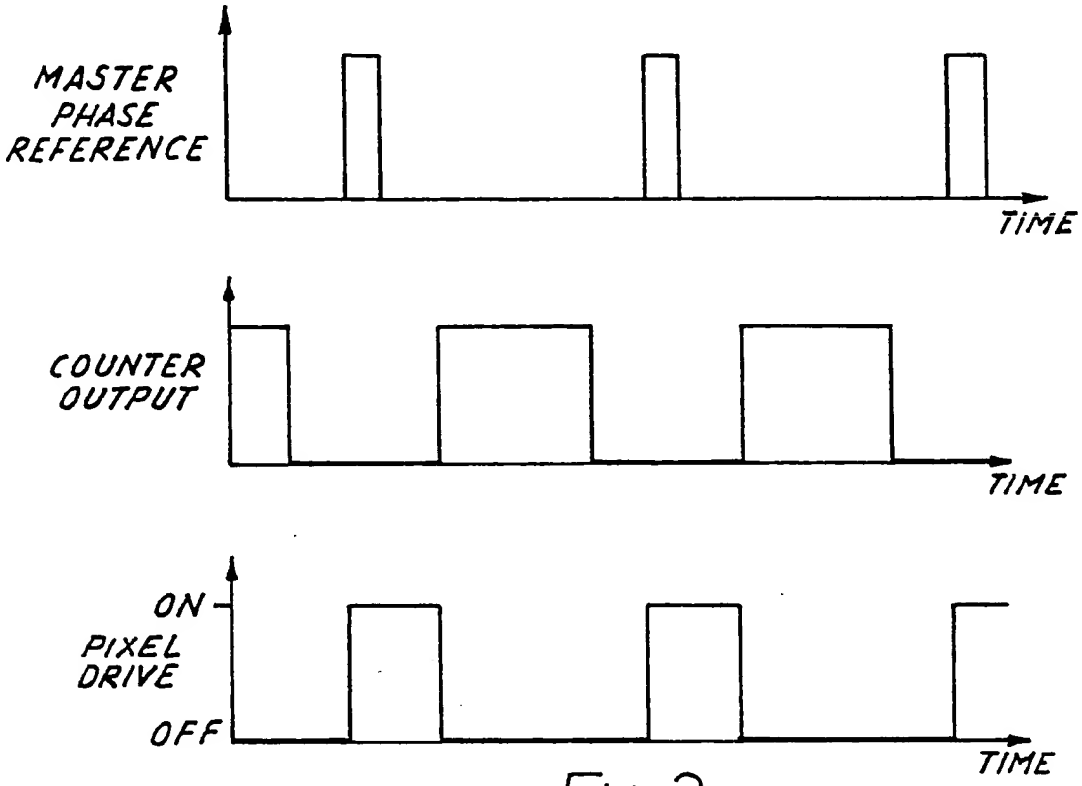

FIG.2

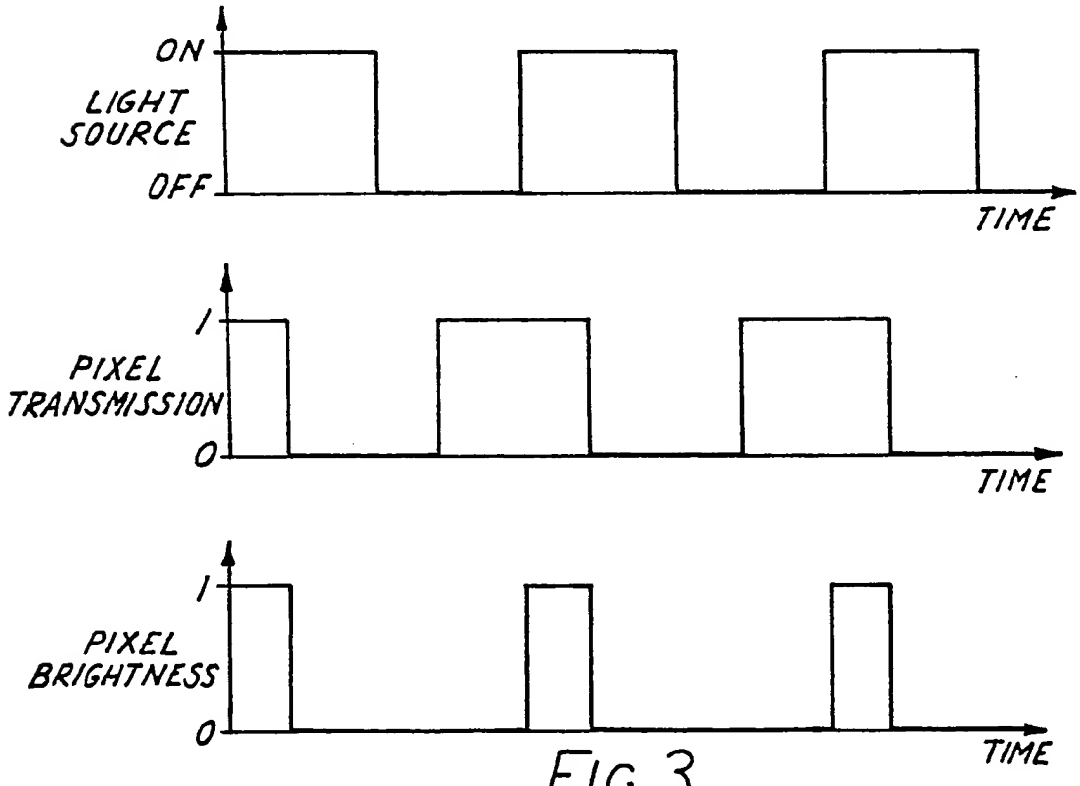

FIG.3

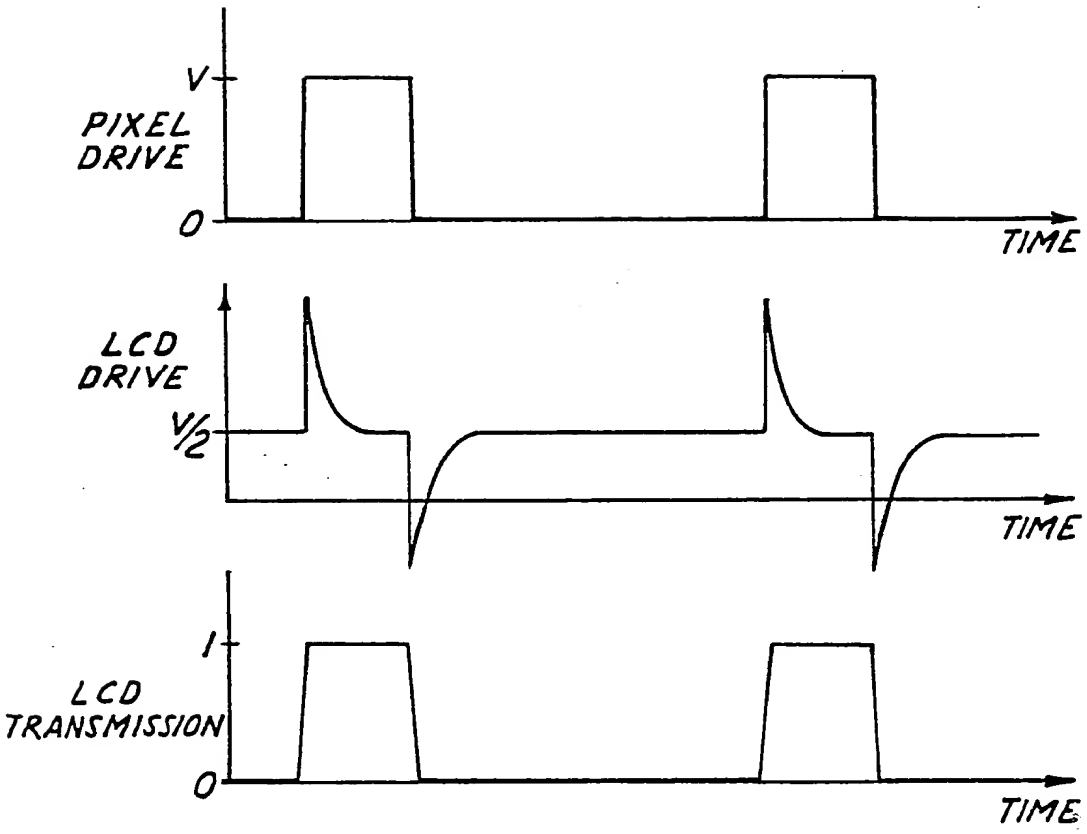
V
PIXEL
DRIVE
0
TIME
LCD
DRIVE
V/2
TIME
1
LCD
TRANSMISSION
0
TIME

FIG. 5

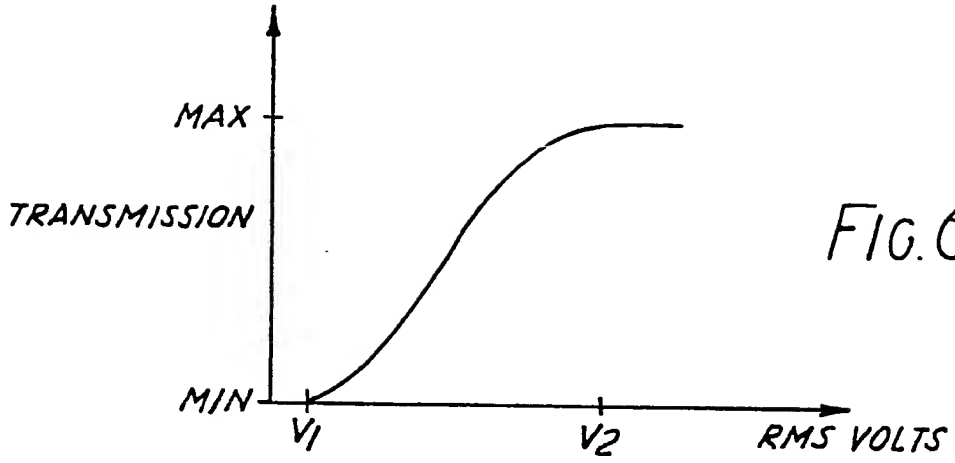

FIG. 6

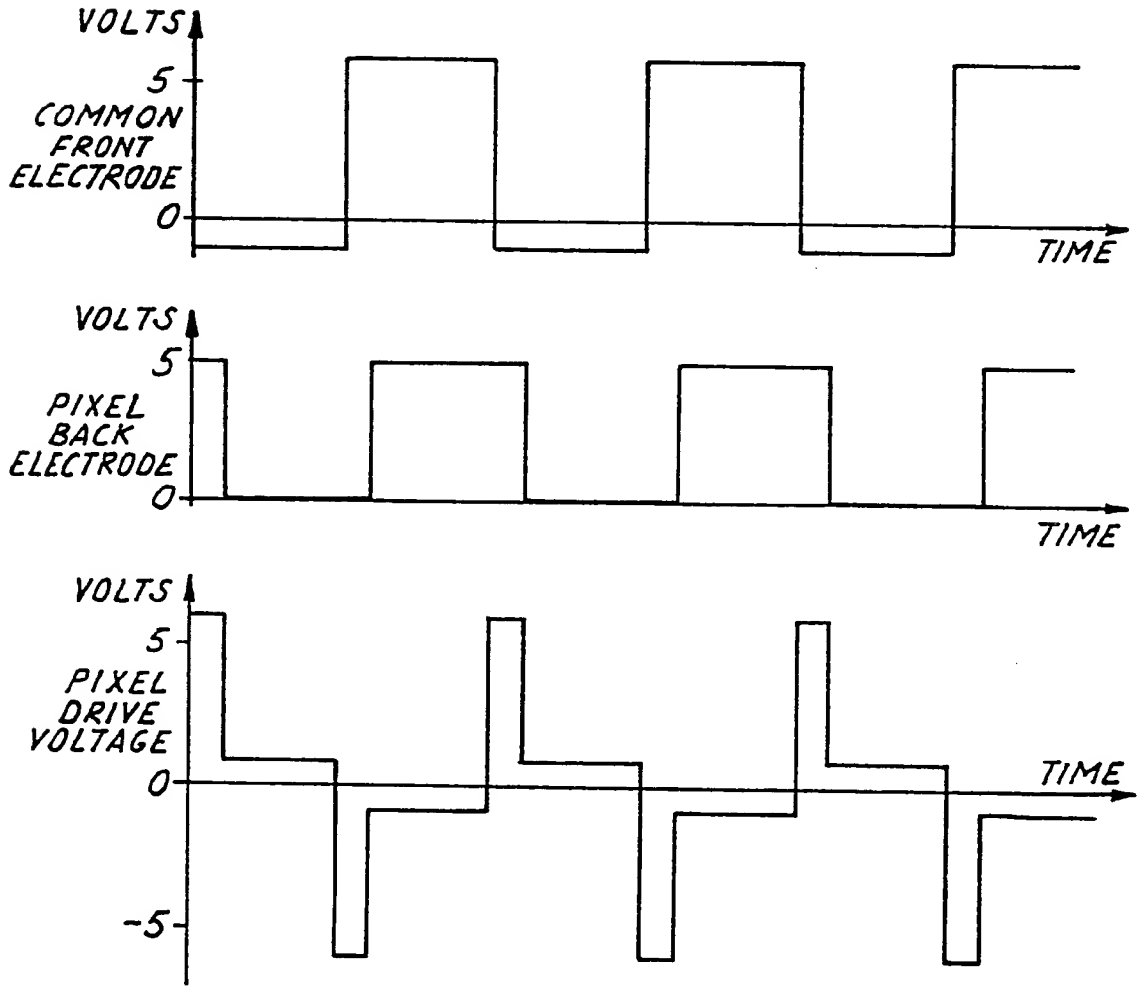

FIG. 7